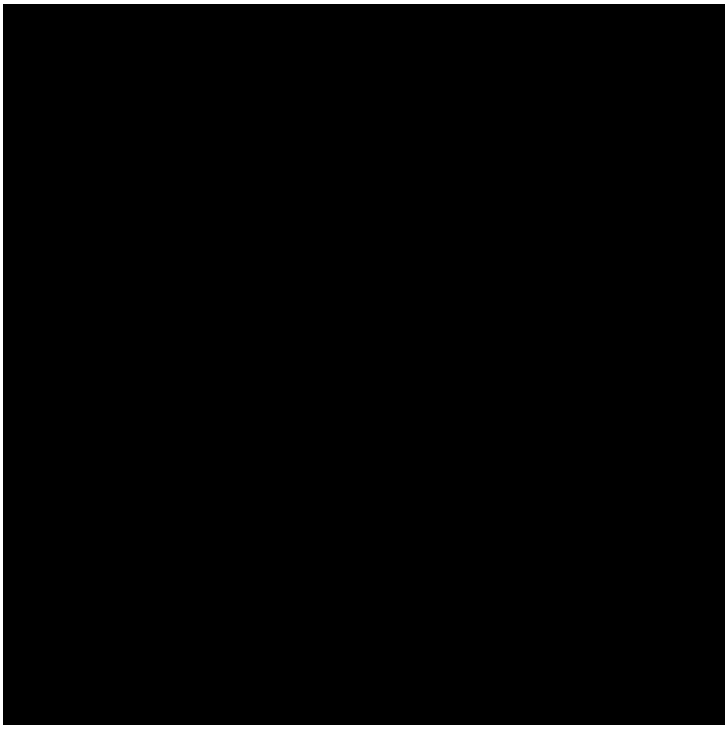
# 74LS11 Triple 3 - Input AND Logic Gate IC - Datasheet

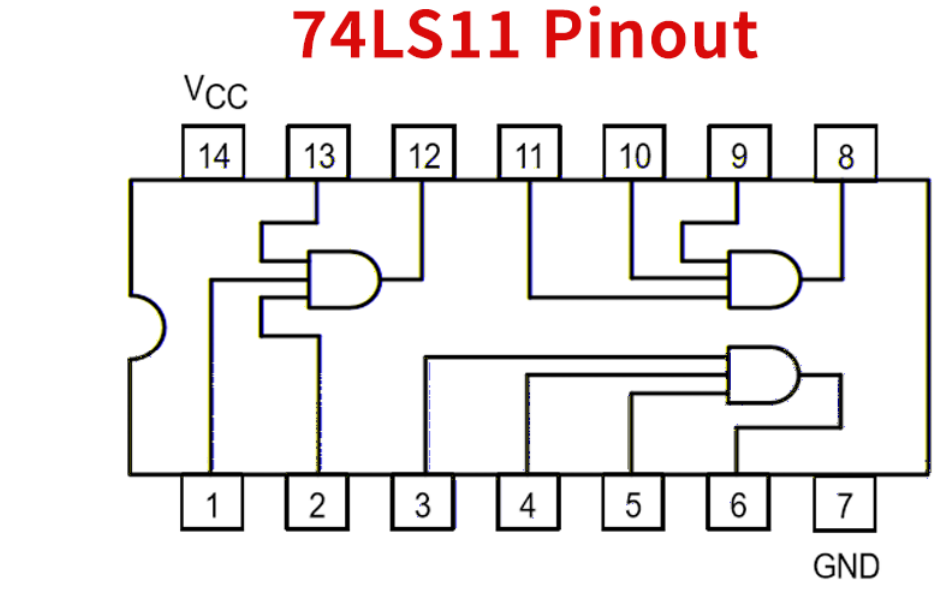
The 74LS11 IC package contains three independent positive logic 3-input AND Gates. It is the part of 74XXYY IC series. The 74LS11 IC has a wide range of working voltage, a wide range of working conditions, and directly interfaces with CMOS, NMOS, and TTL. The output of the IC always comes in TTL which makes it easy to work with other TTL devices and microcontrollers. The IC 74LS11 is smaller in size and it has a much faster speed which makes it reliable in every kind of device.



## What is an AND Gate?

An AND Gate is a logical operator/circuit that gives a logical high (1) output only when all of its inputs are high (1), otherwise, it results in a logical low (0). The logic or Boolean expression for a digital logic AND gate is that for Logical Multiplication which is denoted by a single dot or full stop symbol ( . ).

### 74LS11 Pinout




### 74LS11 Pin Configuration

Pin NoPin NameDescription1A1INPUT 1 of GATE 12B1INPUT 2 of GATE 13A2INPUT 1 of GATE 24B2INPUT 2 of GATE 25C2INPUT 3 of GATE 26Y2OUTPUT of GATE 27GNDGround8Y3OUTPUT of GATE 39A3INPUT 1 of GATE 310B3INPUT 2 of GATE 311C3INPUT 3 of GATE 312Y1OUTPUT of GATE 113C1INPUT 3 of GATE 114VCCSupply Voltage

## 74LS11 Specifications

- Supply Voltage 7V
- Input Voltage 7V
- Operating Free Air Temperature Range 0°C to +70°C
- Storage Temperature Range -65°C to +150°C
- Maximum current allowed to draw through each gate output: 8mA
- TTL outputs
- Low power consumption
- Typical Rise Time: 18ns
- Typical Fall Time: 18ns

## Applications

- The chip provides TTL outputs that are needed in some systems.
- 74011 IC is usually used in a place where 3 – input logical AND operation is required.
- Also used in devices such as PCs and notebooks.

You can download this Datasheet 74LS11 3-Input AND gate from the link given below:

See Also: 74LS00 Quad Two Input NAND Gate | 7407 Hex Buffer IC | 7404 NOT Gate IC

**Related posts:**

# 74LS11 Triple 3-input AND Gate - Datasheet Hub

The 74LS series of integrated circuits (ICs) was one of the most popular logic families of transistor-transistor logic (TTL) logic chips. 74LS series is a bipolar, low-power Schottky IC. 74LS11 Triple 3-input AND Gate contain three independent 3-input AND Gates

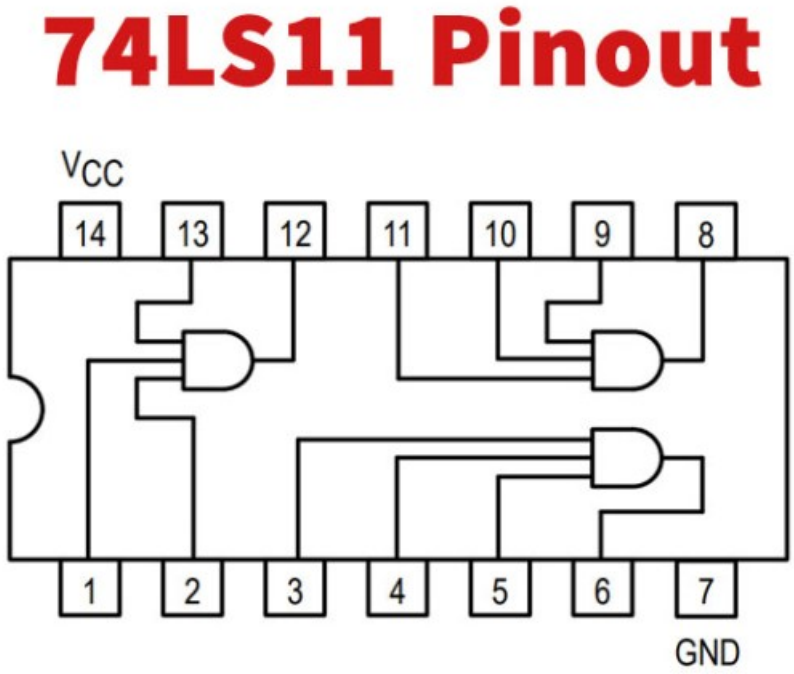
## 74LS11 Features

- Three Independent AND Gates
- Standard Pin Configuration
- Fast Switching Times
- Operating Temperature up to 70°C
- Standard TTL Switching Voltages

## 74LS11 Specifications

Supply Voltage4.75 – 5.25VdcMaximum Clock Frequency40MhzPower Dissipation2mW/gate @100kHzMinimum Output Current8mAPropagation Delay10nSFan Out (TTL Loads)20

## 74LS11 Pinout Diagram




### 74LS11 Pin Description

Pin NoPin NameDescription1A1AND Gate 1 Input 12B1 AND Gate 1 Input 23A2 AND Gate 2 Input 14B2 AND Gate 2 Input 25C2 AND Gate 2 Input 36D2 AND Gate 2 Output 7GNDGround8D3 AND Gate 3 Output 9A3 AND Gate 3 Input 110B3 AND Gate 3 Input 2 11C3 AND Gate 3 Input 312D1 AND Gate 1 Output 13C1 AND Gate 1 Input 3 14VCCPositive Supply

## 74LS11 Circuit

### Applications

- Data transmission control in digital electronics
- Digital measuring instruments
- Alarm circuits

#### 74LS11 Alternative Equivalent

74LS08, 74LS09, 74LS21

Download 74LS11 Triple 3-input AND Gate Datasheet from the link given below.

### Related posts:

# 74LS 3 input AND gate datasheet & applicatoin notes

**rs flip-flop IC 7400**

Abstract: 74ls105 TTL LS 7400 74LS series logic gates 7400 fan-out 74LS 3 input AND gate IC TTL 7400 schematic 74LS04 fan-out 74ls series logic family 90 watts inverter by 12v dc with 6 transisters Text: /7400 functtions where 54LS/ 74LS functions aren't yet available. The low input currents of Low Power , different for 54/ 74LS types than they are for the corresponding 54/74 type. 3 . Use standard 54/74 where it , affected by sim ply plugging in 54/ 74LS . 2. Reduced power supply cost. 3 . Upgrade system capability by , out production. 3 . Inventory - By placing both 54/74 and 54/74L with 54/ 74LS , the total number of , maintaining the same maximum logic " 1" input volt age, therefore noise

margin for 54/ 74LS in the logic " 1

OCR Scan PDF

**74ls Logic Family Specifications**

Abstract: 74LS 74LS136 74Ls signetics 74LS 3 input AND gate Text: voltage level INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A, B Y DESCRIPTION Inputs Output 74LS , unless otherwise noted.) 74LS 7.0 - 0 .5 to +7.0 - 3 0 to +1 -0 .5 to + V c c 0 to 70 UNIT V V mA V °C , efin itio n INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V Rep. Rate 1MHz 1MHz , second. 4. Measure tec with one input of each gate at 4.5V, the other inputs grounded, and all outputs , Signetics 74LS136 Gate Quad Two-Input Exclusive-OR Gate (Open Collector) Product Specification

OCR Scan PDF 74LS136 N74LS136N 10LSul 20/jtA WF07570S F07380S 74ls Logic Family Specifications 74LS 74LS136 74Ls signetics 74LS 3 input AND gate

**74LS266 pin configuration**

Abstract: TTL 74LS266 74ls gate symbols 74Ls signetics 74ls TTL family 74LS 74LS266 N74LS266N 74LS 04 N 74ls Logic Family Specifications Text: Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74LS A, B Inputs 2LSul Y Output 10LSul NOTE: A 74LS unit load (LSul) is 20(iA l(H and -0.4mA l|L. PIN , .) PARAMETER 74LS UNIT Vcc Supply voltage 7.0 V VlN Input voltage -0.5 to +7.0 V 'in Input current -30 to , ï»¿Signetics 74LS266 Gate Logic Products FUNCTION TABLE H = HIGH voltage level L = LOW voltage level Quad 2-lnput Exclusive-NOR Gate (Open Collector) Product Specification TYPE TYPICAL PROPAGATION

OCR Scan PDF 74LS266 74LS266 N74LS266N 10LSul 500ns 74LS266 pin configuration TTL 74LS266 74ls gate symbols 74Ls signetics 74ls TTL family 74LS N74LS266N 74LS 04 N 74ls Logic Family Specifications

**74ls gate symbols**

Abstract: 74ls Logic Family Specifications 74ls TTL family 74ls signetics 74LS 74LS136 N74LS136N Text: Logic Products Product Specification Gate 74LS136 PARAMETER 74LS UNIT Vcc Supply voltage 7.0 V V , Outputs VM - 1,3V for 74LS ; VM - 1.5V for all other TTL families. Input Pulse Definition DEFINITIONS Rl , . Measure Icc with one input of each gate at 4.5V, the other inputs grounded, and all outputs open. AC , OUTPUT 74LS136 Gate Quad Two-Input Exclusive-OR Gate (Open Collector) Product Specification TYPE , devices processed to Military Specifications, see the Signetics Military Products Data Manual. INPUT AND

OCR Scan PDF 74LS136 74LS136 N74LS136N 10LSul 20fiA wf07s70s wfo750os 74ls gate symbols 74ls Logic Family Specifications 74ls TTL family 74ls signetics 74LS N74LS136N

**74ls gate symbols**

Abstract: 74LS01 function table 74LS01 74ls TTL family 1N3064 1N916 74LS N74LS01D N74LS01N 74ls01 SIGNETICS Text: . INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74LS A, B Inputs 1LSul Y Output ipi-Sul , range unless otherwise noted.) PARAMETER 74LS UNIT Vcc Supply voltage 7.0 V Vin Input voltage -0.5 , PARAMETER 74LS UNIT Min Nom Max Vcc Supply voltage 4.75 5.0 5.25 V V]H HIGH-level input voltage 2.0 , than or equal to the table entries. VM = 1,3V for 74ls ; VM = 1.5V for all other TTL families. Input , ï»¿Signetics 74LS01 Gate Logic Products Quad Two-Input NAND Gate (Open Collector) Product

OCR Scan PDF 74LS01 74LS01 N74LS01N N74LS01D 20/xA 74ls gate symbols 74LS01 function table 74ls TTL family 1N3064 1N916 74LS N74LS01D N74LS01N 74ls01 SIGNETICS

**74LS54**

Abstract: No abstract text available Text: ecification Gate 74LS54 ABSOLUTE MAXIMUM RATINGS Supply voltage Input voltage Input current (Over operating free-air temperature range unless otherwise noted.) 74LS 7.0 - 0 .5 to +7.0 - 3 0 to +1 -0 .5 to + , Signetics 74LS54 Gate Four-Wide Two- & Three-Input AND-OR-lnvert Gate Product Specification , ; T a = 0°C to +70°C N74LS54N N74LS54D INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A -K Y NOTE: Where a 74-LS unit load (LSul) is 20 # jA l!H and -0 .4 m A l|L. FUNCTION TABLE INPUTS A H X

OCR Scan PDF 74LS54 N74LS54N N74LS54D 74-LS F07S70S 74LS54

**74156**

Abstract: 74ls gate symbols 74LS156 SIGNETICS 74156 demultiplexer signetics 1N3064 1N916 74LS 74LS156 LS156 N74156N Text: Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74 74LS All , ») (10) f <11)1 (12)1 Vcc - Pin 16 QND - Pin 8 Both decoder sections have a 2- input enable gate . For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input (Ea â¢ Ea). Decoder , temperature range unless otherwise noted.) PARAMETER 74 74LS UNIT Vcc Supply voltage 7.0 7.0 V Vin Input , , Vil = MAX Iol = MAX 0.2 0.4 0.35 0.5 V 'ol = 4mA ( 74LS ) 0.25 0.4 V V|Â« Input clamp voltage

OCR Scan PDF LS156 1N916, 1N3064, 500ns 74156 74ls gate symbols 74LS156 SIGNETICS 74156 demultiplexer signetics 1N3064 1N916 74LS 74LS156 LS156 N74156N

**74LS266 pin configuration**

Abstract: TTL 74LS266 74ls Logic Family Specifications 74LS 74Ls signetics Text: Signetics 74LS266 Gate Quad 2- Input Exclusive-NOR Gate (Open Collector) Product Specification , Operating free-air temperature range 74LS 7.0 -0.5 to +7.0 - 3 0 to +1 -0.5 to +Vcc 0 to 70 UNIT V V mA V °C , one second. 4. Measure Icc with one input of each gate at 4.5V, the other inputs grounded and the , input HIGH December 4, 1985 5-462 Signetics Logic Products Product Specification Gate , %; T a = 0°C to +70°C N74LS266N INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A, B Y NOTE: A

OCR Scan PDF 74LS266 N74LS266N 10LSul 500ns 500ns 74LS266 pin configuration TTL 74LS266 74ls Logic Family Specifications 74LS 74Ls signetics

**TTL 74ls54**

Abstract: 74ls Logic Family Specifications 74LS54 74LS Text: otherwise noted.) 74LS 7.0 -0 .5 to + 7.0 - 3 0 to +1 -0 .5 to +Vcc¡ 0 to 70 UNIT V V mA V °C PARAMETER , the table entries. Input Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S , S ignetics 74LS54 Gate Four-Wide Two- & Three-Input AND-OR-Invert Gate Product Specification , % ; T A = 0°C to +70°C N74LS54N N74LS54D INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A -K Y NOTE: W here a 74LS unit load (LSul) is 20 yA I|h and -0 .4 m A I|L. FUNCTION TABLE INPUTS A H X X

OCR Scan PDF 74LS54 74LS54 N74LS54N N74LS54D F07S70S TTL 74ls54 74ls Logic Family Specifications 74LS

**74LS01**

Abstract: 74LS01 TTL 74LS01 function table IC 74LS WF07570S ttl 74LS01 Text: V|N ·in V OUT 74LS 7.0 -0 .5 to +7.0 - 3 0 to +1 -0.5 to +V Cc 0 to 70 UNIT V V mA V °C , Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V Rep. Rate 1MHz , Signetics | 74LS01 Gate Quad Two-Input NANO Gate (Open Collector) Product Specification , , see the Signetics Military Products Data Manual INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A, B Y DESCRIPTION Inputs Output 74LS 1LSul 10LSul NOTE: Where a 74LS unit load (LSul) is 20juA I|h

OCR Scan PDF 74LS01 N74LS01N N74LS01D 10LSul 20juA WF07570S 74LS01 74LS01 TTL 74LS01 function table IC 74LS WF07570S ttl 74LS01

**74ls gate symbols**

Abstract: 74ls 74ls signetics 74LS136 N74LS136N 74ls Logic Family Specifications Text: 74LS UNIT Vcc Supply voltage 7.0 V VlN Input voltage -0.5 to +7.0 V !|N Input current -30 to +1 mA , =1.3V for 74LS ; VM-1.5V for all other TTL families. Input Pulse Definition FAMILY INPUT PULSE REQUIREMENTS , 'ol = 4mA ( 74LS ) 0.25 0.4 V Vik Input clamp voltage Vcc = MIN, l| = l|k -1.5 V I Input current , . Measure Ice with one input of each gate at 4.5V, the other inputs grounded, and all outputs open. AC , ï»¿Signetics 74LS136 Gate Logic Products Quad Two-Input Exclusive-OR Gate (Open Collector

OCR Scan PDF 74LS136 74LS136 N74LS136N 10LSul 20fiA WF07580S 74ls gate symbols 74ls 74ls signetics N74LS136N 74ls Logic Family Specifications

**TTL 74LS266**

Abstract: No abstract text available Text: Signetics Gate 74LS266 Quad 2- Input Exclusive-NOR Gate (Open Collector) Product , output in HIGH output state Operating free-air temperature range 74LS 7.0 -0 .5 to +7.0 - 3 0 to +1 - , Ice with one input of each gate at 4.5V, the other inputs grounded and the outputs open. AC , INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V Rep. Rate 1MHz 1MHz 1MHz Pulse , , see the Signetics Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A

OCR Scan PDF 74LS266 N74LS266N 10LSul 20/iA 500ns 500ns TTL 74LS266

**74ls gate symbols**

Abstract: 74LS54 1N3064 1N916 74LS N74LS54D N74LS54N 74ls TTL family Text: SO N74LS54D INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74LS A-K Inputs 1LSul Y , noted.) PARAMETER 74LS UNIT Vcc Supply voltage 7.0 V Vin Input voltage -0.5 to +7.0 V 'IN Input , for 74LS ; VM = 1.5V for all olher TTL families. Input Pulse Definition FAMILY INPUT PULSE , ( 74LS ) 0.25 0.4 V V|K Input clamp voltage Vcc = MIN, I, = llK -1.5 V ! Input current at maximum ' , ï»¿Signetics 74LS54 Gate Four-Wide Two- & Three-Input AND-OR-Invert Gate Product Specification

OCR Scan PDF 74LS54 74LS54 N74LS54N N74LS54D 10LSul 20/jA 74ls gate symbols 1N3064 1N916 74LS N74LS54D N74LS54N 74ls TTL family

**74155 demultiplexer pin diagram and function table**

Abstract: 74155 demultiplexer 74155 PIN DIAGRAM 74155 pin configuration 74ls155 pin configuration 74155 decoder LS155 74155 demultiplexer pin configuration decoder 74155 74155 signetics Text: LOGIC DIAGRAM *o *1 Both decoder sections have a 2- input enable gate . For decoder "a " the enable gate re quires one active-HIGH input and one activeLOW input (Ea -Ea ). Decoder "a " can accept either , -0.5 to +Vcc 74LS 7.0 -0.5 to +7.0 - 3 0 to +1 -0.5 to +Vcc UNIT V V mA V °C 0 to 70 December 4 , 4mA ( 74LS ) - 1 .5 Input clamp voitage Input current at maximum input voltage HIGH-level Input , accept the binary weighted Address input (Ao, A i) and provide four mutually exclusive active-LOW outputs

OCR Scan PDF LS155 74LS155 1N916, 1N3064, 500ns 500ns 74155 demultiplexer pin diagram and function table 74155 demultiplexer 74155 PIN DIAGRAM 74155 pin configuration 74ls155 pin configuration 74155 decoder LS155 74155 demultiplexer pin configuration decoder 74155 74155 signetics

**Not Available**

Abstract: No abstract text available Text: Signetics 74LS266 Gate Quad 2- Input Exclusive-NOR Gate (Open Collector) Product Specification , operating free-air temperature range unless otherwise noted.) PARAMETER Vcc 74LS 7.0 -0 .5 to +7.0 - 3 0 , table entries. Input Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V , Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A, B Y DESCRIPTION Inputs Output 74LS 2LSul 10LSul NOTE: A 74LS unit load (LSul) is 20/iA Iih and -0.4m A l|[_. PIN

OCR Scan PDF 74LS266 74LS266 N74LS266N 10LSul 20/iA 500ns 500ns

**Not Available**

Abstract: No abstract text available Text: temperature range unless otherwise noted.) 74LS 7.0 - 0 .5 to +7.0 - 3 0 to +1 - 0.5 to + V qq 0 to 70 UNIT V , Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V Rep. Rate 1MHz , Signetics 74LS01 Gate Quad Two-input NAND Gate (Open Collector) Product Specification Logic , , see the Signetics Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A, B Y DESCRIPTION Inputs Output 74LS 1 LSul 10LSul NOTE: Where a 74LS unit load (LSul) is 20/iA l|H

OCR Scan PDF 74LS01 N74LS01N N74LS01D 10LSul 20/iA F07570S

**74156 demultiplexer**

Abstract: 74LS156 equivalent TTL 74156 74156 74LS156 1N3064 demultiplexer 74ls 74LS LS156 N74LS156D Text: Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74 74LS All , enable gate . For decoder "a" the enable gate requires one active-HIGH input and one active-L.OW input (Ea , and -1.6mA l|L, and a 74LS unit load (LSul) Is 20/iA Iih and -0.4mA l|L. PIN CONFIGURATION E.tl , SYMBOL (IEEE/IEC) 12 13 3 14 15 JÃ TTTT AO E DECODER C Â»1 0 12 3 TTTT 9 10 11 12 LSO&Z&OS Vcc - Pin 16 GND- Pin 8 December 4, 1985 5-275 13 le- 3 ti ' n r 1 Dx 4 0 1 Lti G4 2 3

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**74LS54**

Abstract: 74Ls signetics Text: Input voltage Input current (Over operating free-air temperature range unless otherwise noted.) 74LS , entries. Input Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V , Signetìcs 74LS54 Gate Four-Wide Two- & Three-Input AND-OR-Invert Gate Product Specification , Signetics Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A -K Y DESCRIPTION Inputs Output 74LS 1LSul 10LSul FUNCTION TABLE INPUTS A H X X X B H X X X OUTPUT F X X H X G X

OCR Scan PDF 74LS54 N74LS54N N74LS54D 10LSul WP07570S 74LS54 74Ls signetics

**74ls gate symbols**

Abstract: 74LS266 pin configuration 74LS266 74LS N74LS266N Text: .) PARAMETER 74LS UNIT Vcc Supply voltage 7.0 V Vin Input voltage -0.5 to +7.0 V i|n Input current -30 to , ï»¿Signetics 74LS266 Gate Logic Products FUNCTION TABLE INPUTS H - HIGH voltage level L = LOW voltage level OUTPUT Quad 2-lnput Exclusive-NOR Gate (Open Collector) Product Specification TYPE , devices processed to Military Specifications, see the Signetics Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74LS A, B Inputs 2LSul Y Output 10LSul NOTE: A

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**74155 demultiplexer pin diagram and function table**

Abstract: 74155 pin configuration 74155 demultiplexer 74ls155 pin configuration 74155 decoder pin diagram of 74155 ttl 74155 74155 demultiplexer signetics 74155 PIN DIAGRAM 74155 Text: decoder sections have a 2- input enable gate . For decoder "a" the enable gate requires one active-HIGH , = MAX 0.2 0.4 0.35 0.5 V iol = 4mA ( 74LS ) 0.25 0.4 V ViÂ« Input clamp voltage Vcc = MIN, I , the table entries. VM = 1,3V for 74LS ; VM = 1,5V for ah other TTL families. Input Pulse Definition , . Each decoder section, when enabled, will accept the binary weighted Address input (A0, A-i) and provide , processed to Military Specifications, see the Signetics Military Products Data Manual. INPUT AND OUTPUT

OCR Scan PDF LS155 74LS155w- 1N916, 1N3064. 500ns 74155 demultiplexer pin diagram and function table 74155 pin configuration 74155 demultiplexer 74ls155 pin configuration 74155 decoder pin diagram of 74155 ttl 74155 74155 demultiplexer signetics 74155 PIN DIAGRAM 74155

**TTL 74156**

Abstract: demultiplexer 3 16 ttl 74156 C005970S Text: « *o A1 Both decoder sections have a 2- input enable gate . For decoder " a " the enable gate re , unless otherwise noted.) 74 7.0 -0 .5 to + 5.5 - 3 0 to + 5 -0 .5 to + Vcc 74LS 7.0 -0 .5 to +7.0 - 3 0 to , Address inputs (A0, A,) and provide four mutually exclu sive active-LOW outputs (0 - 3 ). When the enable , Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS All All DESCRIPTION Inputs Outputs 74 1ul 10ul 74LS 1LSul 10LSul NOTE: Where a 74 unit load (ul) is understood to be 40

OCR Scan PDF LS156 74LS156 1N916, 1N3064, 500ns 500ns TTL 74156 demultiplexer 3 16 ttl 74156 C005970S

**74ls gate symbols**

Abstract: 74LS54 74LS N74LS54D N74LS54N Text: ï»¿Signetics Logic Products 74LS54 Gate Four-Wide Two- & Three-Input AND-OR-Invert Gate Product Specification INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74LS A-K Inputs 1LSul Y Output , PARAMETER 74LS UNIT Min Nom Max VCC Supply voltage 4.75 5.0 5.25 V V|h HIGH-level input voltage 2.0 , Military Products Data Manual. FUNCTION TABLE MOTE: Where a 74LS unit load (LSul) is 20jiA l|H and , E n rÂ°Ã¯ 33 Â»cc ni E n n] E Å [I H m m 3 QND (T 3 "Ã¡D-1 ZP*1" â 150S530S 5-93

OCR Scan PDF 74LS54 10LSul N74LS54N N74LS54D 20jiA 74ls gate symbols 74LS N74LS54D N74LS54N

**74ls gate symbols**

Abstract: 74LSC 74ls TTL family 74ls characteristics 74LS family 74ls Logic Family Specifications 74ls01 74LS 74ls signetics 1N3064 Text: . INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74LS A, B Inputs 1LSul Y Output 10LSul , temperature range unless otherwise noted.) PARAMETER 74LS UNIT Vcc Supply voltage 7.0 V VIN Input voltage , PARAMETER 74LS UNIT Min Nom Max Vcc Supply voltage 4.75 5.0 5.25 V V|H HIGH-level input voltage 2.0 , the table entries. VM - 1 3V for 74LS ; VM - 1,5V for all other TTL families. Input Pulse Definition , ï»¿Signetics 74LS01 Gate Logic Products FUNCTION TABLE INPUTS H = HIGH voltage level L - LOW

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**74LS266N**

Abstract: IC PIN CONFIGURATION OF 74LS266 74LS266 Text: Signetics 74LS266 Gate Quad 2- Input Exclusive-NOR Gate (Open Collector) Product Specification , noted.) PARAMETER v cc VIN l|N VouT Ta 74LS 7.0 - 0 . 5 to + 7 . 0 - 3 0 to + 1 - 0 . 5 to + V c , input of each gate at 4.5V, the other inputs grounded and the outputs open. AC ELECTRICAL CH A RA , . Input Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V Rep , Specifications, see the Signetics Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

OCR Scan PDF 74LS266 74LS266N 10LSul 20/iA 500ns 500ns 74LS266N IC PIN CONFIGURATION OF 74LS266 74LS266

**74LS01 function table**

Abstract: No abstract text available Text: temperature range unless otherwise noted.) PARAMETER Vcc V|N l|N Vqu T Ta 74LS 7.0 -0 .5 to +7 .0 - 3 , H L Input Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V , Signefics 74LS01 Gate Quad Two-Input NAND Gate (Open Collector) Product Specification Logic , , see the Signetics Military Products Data Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS A, B Y NOTE: Where a 74LS unit load (LSul) is 20 /jA Iih and -0 .4 m A lj|_. DESCRIPTION

OCR Scan PDF 74LS01 N74LS01N N74LS01D WF07570S 74LS01 function table

# 74LS series logic gates 3 input or gate datasheet & applicatoin

# notes

**rs flip-flop IC 7400**

Abstract: 74ls105 TTL LS 7400 74LS series logic gates 7400 fan-out 74LS 3 input AND gate IC TTL 7400 schematic 74LS04 fan-out 74ls series logic family 90 watts inverter by 12v dc with 6 transisters Text: maintaining the same maximum logic " 1" input volt age, therefore noise margin for 54/ 74LS in the logic " 1 , families. TABLE 9 FANOUT (0°-70°C) LOGIC 1/ LOGIC 0 DRIVING GATES 74 74 74L 74LS DRIVEN GATES 10/10 40/89 , .) The buffer gate (54/7440) is capable of sinking current or supplying cur rent to 30 loads (N = 30). , 1 o u tp u t a t a tim e. S54 Series 54/74 Logic Family The 54/74XX logic family is medium speed , volts below ground, even if -12mA of current is drawn. DESIGN CONSIDERATIONS Logic Definition Series

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**74ls gate symbols**

Abstract: 74LS series logic gate symbols 74LS series logic gates 74LS logic gates oc 44 74LS TTL series 74LS D-32 buffer 74ls series logic gates 74LS AND GATE Text: Schottky 54S/74S 3 ns/19 mW L o w Power Schottky 54LS/ 74LS 5 ns/2 mW ~c g o c 3 li. < 0 S > o> (S , - - D94 3I,6A,9A AND-OR Gates 2 3 D ual 4-2 In p u t 2 -2-2-3 In p u t (Exp) - - - , 3I,6A,9A 3I,6A,9A Gate Expanders 13 14 15 T rip le 3 -In p u t D ual 4 -In p u t 2 -2-3-3 A N D , ,9B 4L,6B,9B 1. OC = open collector, 3S = 3 -state. 2. The logic symbols located in the Logic /Connection Diagram Section are for the DIP version. 3 . For specific availability or delivery information on a

OCR Scan PDF ns/10 54H/74H ns/22 54S/74S ns/19 54LS/74LS 74LS266 /74LS 74ls gate symbols 74LS series logic gate symbols 74LS series logic gates 74LS logic gates oc 44 74LS TTL series 74LS D-32 buffer 74ls series logic gates 74LS AND GATE

**74LS02 gate diagram**

Abstract: TTL 74ls02 74LS02 truth table IC TTL 74LS02 74LS02 pinout T43CA 74LS02 LC74HC02 LC74HC02M IC 74LS02 Text: High-Speed Standard Logic LC74HC Series Quad 2- Input NOR Gate Â©2139A Features â¢ The LC74HC02M consists of 4 identical 2- input NOR gates . â¢ Uses CMOS silicon gate process technology to achieve , High-Speed Standard Logic 3003A LC74HC Series Quad 2-lnput NOR Gate Â©16958 Features The LC74HC02 consists of 4 identical 2- input NOR gates . Uses CMOS silicon gate process technology to achieve operating , Quad 2- Input NOR Gate Â©2139A Features â¢ The LC74HC02M consists of 4 identical 2- input NOR gates

OCR Scan PDF QQQEb04 LC74HC02M LC74HC LC74HC02M 74LS02) 54LS/74LS-TTL Tas85Â 10sec LC74HC02M) 74LS02 gate diagram TTL 74ls02 74LS02 truth table IC TTL 74LS02 74LS02 pinout T43CA 74LS02 LC74HC02 IC 74LS02

**74h541**

Abstract: 74LS series nand gates SN7423 4 input nor gate 7423 ic 7423 g 106IC Text: tested separately. B. W hen testing A N D - O R - I N V E R T or A N D - O R gates , each A N D gate is , SERIES 54/74, 54H/74H, 541/741. 54LS/ 74LS , 54S/74S TRANSISTOR-TRAÄSIST0 R LOGIC PARAMETER MEASUREMENT , and Not«) - 1 T O T E M -P O L E O UTPUTS >OH VOH TEST TABLE FUNCTION NAND AND NOR OR INPUT , testing A N D - O R - I N V E R T o r A N D - O R gates , each A N D gate i« tested separately w ith Inputs , TABLE FUNCTION NAND AND NOR OR ^ A N D -O R -IN V E R T A N D -O R NOTE: V CC INPUT CONDITIONS A

OCR Scan PDF 54H/74H, 54L/74L, 54LS/74LS, 54S/74S 106IC 74h541 74LS series nand gates SN7423 4 input nor gate 7423 ic 7423 g 106IC

**74LS series logic gates**

Abstract: 74LS series logic gates 3 input or gate buffer 74ls series logic gates 54LS 74LS N74LS670 S54LS670 Text: ï»¿SPEED/PACKAGE AVAILABILITY 54LS F,W 74LS A SWITCHING CHARACTERISTICS v cc = 5V, T. FUNCTION TABLE PIN CONFIGURATION (EACH GATE ) INPUTS OUTPUT A B L L L L H H H L H H H L H = high level L = low level 25Â°C FROM LIMITS PARAMETER* ( INPUT ) TEST CONDITIONS MIN TYP MAX UNIT lPLH *PHL 'PLH 'PHL A or B A or B Other input low Other input high CL = 15pF, Rl = 2kfi 10 10 10 10 23 17 , are buffered to lower the drive requirements to one Series 54LS/ 74LS standard load, and input-clamping

OCR Scan PDF S54LS670 N74LS670 16-bit 54LS/74LS 74LS series logic gates 74LS series logic gates 3 input or gate buffer 74ls series logic gates 54LS 74LS

**Not Available**

Abstract: No abstract text available Text: SignelÃ¬cs 7451, LS51, S51 Gates '51, S51 Dual 2-Wide 2- Input AND-OR-lnvert Gate LS51 Dual 2-Wlde 3-Input , 2-Wide 2- Input AND-OR-lnvert Gate Product Specification Logic Products TYPICAL , /IEC) 853-0564 81501 Product Specification Signetics Logic Products Gates 7451, LS51 , Input voltage -0.5 to +5.5 -0.5 to +7.0 -0 .5 to +5.5 V l|N Input current - 3 0 to , Logic Products Gates 7451, LS51, S51 DC ELECTRICAL CHARACTERISTICS (Over recommended operating

OCR Scan PDF 74LS51 74S51 WF07570S 280ii

**1995 - ic mm74hc**

Abstract: MM74HC 74HC inverter tri-state output ic cd4000 CMOS TTL Logic Family Specifications AL 5052 CD4000 74LS SERIES cmos logic data Difference between LS, HC, HCT devices unbuffered cmos logic application note Text: to output Also the output impedance of an unbuffered gate may change with input logic level voltage , With VCC e 5V these input levels are 3 5V for minimum logic ``1'' (VIH) and 1 0V for a logic ``0'' , 5 (b) FIGURE 3 Input Output Transfer Characteristics for (a) 'HC00 and (b) 'LS00 Nand Gate , feedback capacitance effects When comparing MM54HC MM74HC input currents to TTL logic 54LS 74LS does need , between logic families In order to familiarize the user with the MM54HC MM74HC logic family its input

Original PDF MM54HC MM74HC CD4000 MM54C MM74C MM54HCT MM74HCT MM54HC MM74HC ic mm74hc 74HC inverter tri-state output ic cd4000 CMOS TTL Logic Family Specifications AL 5052 74LS SERIES cmos logic data Difference between LS, HC, HCT devices unbuffered cmos logic application note

**1998 - internal structure 74LS00 nand gate**

Abstract: MM74HC ic mm74hc IC TTL 74LS00 CD4000 FAIRCHILD MM74HC AN-313 mm74c CMOS TTL Logic Family Specifications CD4000 NAND Text: /Output Transfer Characteristics for (b) LS00 Nand Gate The input and output logic voltages and their , ) HC00 www.fairchildsemi.com 2 When comparing MM74HC input currents to TTL logic , 74LS does , logic families. In order to familiarize the user with the MM74HC logic family, its input and output , several stages from input to output. Also, the output impedance of an unbuffered gate may change with input logic level voltage and input logic combination, whereas buffered outputs are unaffected by input

Original PDF MM74HC CD4000 MM74C MM74HCT MM74HC internal structure 74LS00 nand gate ic mm74hc IC TTL 74LS00 FAIRCHILD MM74HC AN-313 CMOS TTL Logic Family Specifications CD4000 NAND

**7451 pin configuration of logic circuit**

Abstract: No abstract text available Text: Signetics 7451, LS51, S51 Gates '51, S51 Dual 2-Wide 2- Input AND-OR-Invert Gate LS51 Dual 2-Wlde 3-Input , 2-Wlde 2- Input AND-OR-Invert Gate Logic Products Product Specification FUNCTION , Inputs Output 74 lul 10ul 74S 1Sul 10Sul 74LS 1LSul 10LSul PIN CONFIGURATION LS51 LOGIC , .5 to + V c c 74LS 7.0 -0.5 to +7.0 - 3 0 to +1 -0 .5 to + V Cc 0 to 70 74S 7.0 -0.5 to +5.5 - 3 , equivalent. tjLH> tTHi Values should be less than or equal to the table entries. Input Pulse Definition

OCR Scan PDF 74LS51 74S51 N7451N, N74LS51N, N74S51N N74LS51D, N74S51D 7451 pin configuration of logic circuit

**7451 pin configuration of logic circuit**

Abstract: D1111 74ls gate symbols 1N916 74LS 74LS51 74S51 LS51 N7451N N74LS51D Text: ï»¿Signetics 7451, LS51, S51 Gates Logic Products '51, 'S51 Dual 2-Wide 2-lnput AND-OR-lnvert Gate 'LS51 Dual 2-Wide 3 -lnput, 2-Wide 2-lnput AND-OR-lnvert Gate Product Specification FUNCTION , Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74 74S 74LS Ail Inputs 1 ul 1Sul , Its Respective Manufacturer Signetics Logic Products Product Specification Gates 7451, LS51, S51 , 74LS 74S UNIT Vcc Supply voltage 7.0 7.0 7.0 V Vim Input voltage -0.5 to +5.5 -0.5 to +7.0 -0.5 to

OCR Scan PDF 74LS51 74S51 N7451N, N74LS51N, N74S51N N74LS51D, N74S51D WF07570S 400ft 7451 pin configuration of logic circuit D1111 74ls gate symbols 1N916 74LS LS51 N7451N N74LS51D

**1998 - octal Bilateral Switches**

Abstract: MM74HC14M MM74HC138M CD4025BCM MM74HC00M MM74HC74AM MM74HC125M MM74HC04M cd4046bcm cd4052bcm Text: TO 74F SERIES Gates & Inverters 74AC00SC Quad 2- Input NAND Gate 74AC02SC Quad 2- Input NOR Gate , 0.25 Gates & Inverters CD4001BCM Quad 2- Input NOR/NAND Buffered B Series Gate CD4002BCM Dual 4- Input , Inverter CD4011BCM Quad 2- Input NOR/NAND Buffered B Series Gate CD4023BCM Buffered Triple 3-Input NAND/NOR , EXCLUSIVE-OR Gate CD4071BCM Quad 2- Input OR /AND Buffered B Series Gate CD4081BCM Quad 2- Input OR /AND Buffered B , 0.48 0.28 Gates & Inverters MM74HC00M Quad 2- Input NAND Gate MM74HC02M Quad 2- Input NOR Gate MM74HC04M

Original PDF MM74HC MM74HC00M MM74HC02M MM74HC04M MM74HC08M MM74HC14M MM74HC32M MM74HC86M MM74HC132M MM74HC74AM octal Bilateral Switches MM74HC138M CD4025BCM MM74HC125M cd4046bcm cd4052bcm

**74LS09**

Abstract: 74ls gate symbols 74LS09 ttl 1N3064 1N916 74LS N74LS09N 74LS gates 74ls signetics 74LS logic gates Text: ï»¿Signetics 74LS09 Gates Logic Products FUNCTION TABLE H - HIGH voltage level L = LOW voltage , LOGIC SYMBOL do* LOGIC SYMBOL (IEEE/IEC) _1 _2 IO 3 _ _4 _S S_ _9 10 8_ _12 13 11 , Signetics Logic Products Product Specification Gates 74LS09 ABSOLUTE MAXIMUM RATINGS (Over operating , CONDITIONS PARAMETER 74LS UNIT Min Nom Max Vcc Supply voltage 4.75 5.0 5.25 V V|H HIGH-level input , should be less than or equal to the table entries. VM = 1.3V ( or 74LS ; VM = 1.5V for all other TTL

OCR Scan PDF 74LS09 74LS09 N74LS09N 10LSul 20jjA WF07S80S 74ls gate symbols 74LS09 ttl 1N3064 1N916 74LS N74LS09N 74LS gates 74ls signetics 74LS logic gates

**TTL LS 7413**

Abstract: schmitt trigger 7413 equivalent for 7413 dual schmitt trigger ls 7413 n N74LS13N equivalent for 74LS13 74ls gate symbols 7413 4-input nand gate LS13 1N916 Text: ï»¿Signetics Logic Products DESCRIPTION The '13 contains two 4- input NAND gates which accept , noise margin than conventional NAND gates . Each circuit contains a 4- input Schmitt trigger followed by , positive voltage than Vt+ MAx, the gate will respond in the transitions of the other input as shown in , . INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74 74LS All Inputs 1ul 1 LSul Y Output , otherwise noted.) PARAMETER 74 74LS UNIT Vcc Supply voltage 7.0 7.0 V V,N Input voltage -0.5 to +5.5

OCR Scan PDF

**schmitt trigger 7413**

Abstract: 7413 4-input nand gate equivalent for 7413 dual schmitt trigger 74LS13 function table 74ls gate symbols 1N3064 1N916 74LS 74LS13 LS13 Text: ï»¿Signetics 7413, LS13 Gates Logic Products Dual 4-lnput NAND Schmitt Trigger Product Specification DESCRIPTION The '13 contains two 4- input NAND gates which accept standard TTL input signals and , NAND gates . Each circuit contains a 4- input Schmitt trigger followed by a Darlington level shifter and , Material Copyrighted By Its Respective Manufacturer Signetics Logic Products Product Specification Gates , .) PARAMETER 74 74LS UNIT Vcc Supply voltage 7.0 7.0 V VlN Input voltage -0.5 to +5.5 -0.5 to +7.0 V l|N

OCR Scan PDF

**schmitt trigger 7413**

Abstract: equivalent for 74LS13 PIN CONFIGURATION 74ls13 equivalent for 7413 dual schmitt trigger 7413 4-input nand gate 853051 ttl 7413 Text: Signetics 7413, LS13 Gates Dual 4- Input NAND Schmitt Trigger Product Specification Logic Products DESCRIPTION The ' 13 contains two 4- input NAND gates which accept standard TTL input signals , Logic Products Product Specification Gates 7413, LSI 3 AC ELECTRICAL CHARACTERISTICS ta , conventional NAND gates . Each circuit contains a 4- input Schmitt trigger followed by a Darlington level shifter , . INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS All Y DESCRIPTION Inputs Output 74 1ul 10ut 74LS 1LSuf

OCR Scan PDF

**74LS272**

Abstract: 74LS series logic gates HD74LS 74ALS SERIES ic ttl 74ls 74ls gate symbols 74LS series logic gates 3 input or gate HD74ALS00 ECL IC NAND HD74ALS03 Text: Quadruple 2- input Positive NAND GatÂ« Quadruple 2- input Positive NAND Gates (with open collector outputs) Quadruple 2- input Positive NAND Gates (with open collector outputs) Hex Inverters Hex Inverters (with open collector outputs) Quadruple 2- input Positive AND Gates Quadruple 2- input Positive AND Gates (with open collector output) Dual 4- input Positive NAND Gates Dual 4- input Positive AND Gates Dual D-type , applies between inputs that go directly into the same AND or NAND gate in the functional block diagram

OCR Scan PDF HD74ALS HD74ALS00 HD74ALS01 HD74ALS03 HD74ALS04J HD74ALS05 HD74ALS08 HD74ALS09 HD74ALS20 HD74ALS21 74LS272 74LS series logic gates HD74LS 74ALS SERIES ic ttl 74ls 74ls gate symbols 74LS series logic gates 3 input or gate ECL IC NAND HD74ALS03

**74ls gate symbols**

Abstract: 74LS09 equal 74LS09 function table 74LS09 74LS logic gates 74LS09 N 74LS09 ttl 1N3064 1N916 74LS Text: Gates Quad Two-Input AND Gate (Open Collector) Product Specification TYPE TYPICAL PROPAGATION DELAY , Respective Manufacturer 853-0451 81501 Signetics Logic Products Product Specification Gates 74LS09 , 74LS UNIT Vcc Supply voltage 7.0 V V|n Input voltage -0.5 to +7.0 V l|n Input current -30 to +1 , 74LS ; VM - 1.5V tor all other TTL families. input Pulse Definition FAMILY INPUT PULSE REQUIREMENTS , Manufacturer Signetics Logic Products_Product Specification Gates 74LS09 DC ELECTRICAL CHARACTERISTICS

OCR Scan PDF 74LS09 74LS09 N74LS09N 10LSul 20/uA WF07S80S 74ls gate symbols 74LS09 equal 74LS09 function table 74LS logic gates 74LS09 N 74LS09 ttl 1N3064 1N916 74LS

**TTL 7421**

Abstract: 7421 ttl AND gate 7421 pin configuration PIN CONFIGURATION 7420 TTL 7420 logic gate 7421 AND 74LS20 PIN CONFIGURATION 7420 pin configuration 7420 SIGNETICS TTL 74LS20 Text: ï»¿Signetics I 7420, 7421, LS20, LS21, S20 Gates Dual Four-Input NAND ( 20) AND ('21) Gate Logic , Manufacturer 853-0546 81501 Signetics Logic Products Gates Product Specification 7420, 7421, LS20, LS21 , less than or equal to the table entries. VM- 1.3V ( or 74LS ; Vu - 1.5V for all other TTL families , Manufacturer Signetics Logic Products Product Specification Gates AC ELECTRICAL CHARACTERISTICS ta = 25Â , 8mA 74LS20 10ns 0.8mA 74S20 3 ns 8mA 7421 12ns 8mA 74LS21 9ns 1.7mA ORDERING CODE FUNCTION TABLE

OCR Scan PDF 74LS20 74S20 74LS21 N7420N, N74LS20N, N74S20N N7421N, N74LS21N N74LS20D, N74S20D, TTL 7421 7421

ttl AND gate 7421 pin configuration PIN CONFIGURATION 7420 TTL 7420 logic gate 7421 AND 74LS20 PIN CONFIGURATION 7420 pin configuration 7420 SIGNETICS TTL 74LS20

**7427 pin configuration**

Abstract: TTL 7427 CI 74LS27 TTL 7427 NOR propagation delay TTL 74ls27 IC 7427 74LS27 function table ci 7427 LS27 pin configuration of 7427 Text: Signetics I 7427, LS27 Gates Triple Three-Input NOR Gate Product Specification Logic , Signetics Logic Products Product Specification Gates 7427, LS27 ABSOLUTE MAXIMUM RATINGS , to + 5.5 - 3 0 to + 5 -0 .5 to + V c c 0 to 70 74LS 7.0 - 0 .5 to +7.0 - 3 0 to +1 -0 .5 to + V ( x , the table entries- Input Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S , 2.5ns December 4, 1985 5-56 Signetics Logic Products Product Specification Gates 7427

OCR Scan PDF 74LS27 N7427N, N74LS27N N74LS27D 10LSul WF07570S 7427 pin configuration TTL 7427 CI 74LS27 TTL 7427 NOR propagation delay TTL 74ls27 IC 7427 74LS27 function table ci 7427 LS27 pin configuration of 7427

**TTL 7486**

Abstract: 7486 TTL 7486 PIN CONFIGURATION pin configuration of 7486 7486 7486 signetics pin configuration 7486 LS86 74ls gate symbols 74ls ttl 132 Text: ï»¿Signetics I 7486, LS86, S86 Gates Logic Products Quad Two-Input Exclusive-OR Gate Product , -2.0mA l,Ll and a 74LS unit load (LSul) is 20/uA l,H and -0.4mA l,L. PIN CONFIGURATION LOGIC SYMBOL , Respective Manufacturer Signetics Logic Products Product Specification Gates 7486, LS86, S86 ABSOLUTE , 74LS ; vm = 1 5V for all other TTL families Input Pulse Definition FAMILY INPUT PULSE REQUIREMENTS , Manufacturer Signetics Logic Products Product Specification Gates 7486, LS86, S86 DC ELECTRICAL

OCR Scan PDF 74LS86 74S86 N7486N, N74LS86N, N74S86N N74LS86D, N74S86D 10Sul 10LSul WF07580S TTL 7486 7486 TTL 7486 PIN CONFIGURATION pin configuration of 7486 7486 7486 signetics pin configuration 7486 LS86 74ls gate symbols 74ls ttl 132

**ttl 7486**

Abstract: 7486 pin configuration TTL 7486 AND propagation delay 7486 TTL pin configuration 7486 74LS86 fan-out 7486 signetics pin configuration of 7486 7486 signetics TTL TTL 74ls86 Text: Signetics I 7486, LS86, S86 Gates Quad Two-Input Exclusive-OR Gate Product Specification , 1ul 10ul 74S 1Sul 10Sul 74LS 1LSul 10LSul PIN CONFIGURATION LOGIC SYMBOL LOGIC SYMBOL , .) 74 7.0 -0 .5 to +5.5 - 3 0 to + 5 - 0 .5 to + V Cc 74LS 7.0 - 0 .5 to +7.0 - 3 0 to +1 -0 .5 to + V cq , , 1N3064, or equivalent. tjLH- tjHL Values should be less than or equal to the table entries. Input Pulse Definition INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V Rep. Rate 1MHz

OCR Scan PDF 74LS86 74S86 N7486N, N74LS86N, N74S86N N74LS86D, N74S86D F07570S ttl 7486 7486 pin configuration TTL 7486 AND propagation delay 7486 TTL pin configuration 7486 74LS86 fan-out 7486 signetics pin configuration of 7486 7486 signetics TTL TTL 74ls86

**PIN CONFIGURATION OF 74LS30**

Abstract: TTL 7430 7430 pin configuration 7430 7430 Eight-Input NAND Gate IC 7430 74ls30 equivalent Text: Signetics | 7430, LS30 Gates Eight-Input NAND Gate Product Specification Logic Products , SYMBOL LOGIC SYMBOL (IEEE/IEC) 1 2 3 4 5 6 11 12 & S05400S December 4, 1985 5-61 853-0554 81501 Signetics Logic Products Product Specification Gates 7430, LS30 ABSOLUTE , noted.) 74 7.0 - 0 .5 to +5.5 - 3 0 to + 5 - 0 .5 to + Vcc 0 to 70 74LS 7.0 -0 .5 to +7 .0 - 3 0 to +1 - , Pulse D efin itio n INPUT PULSE REQUIREMENTS FAMILY Amplitude 74 74LS 74S 3.0V 3.0V 3.0V Rep. Rate 1MHz

OCR Scan PDF 74LS30 N7430N, N74LS30N N74LS30D PIN CONFIGURATION OF 74LS30 TTL 7430 7430 pin configuration 7430 7430 Eight-Input NAND Gate IC 7430 74ls30 equivalent

**ttl 7432**

Abstract: 7432 ttl 7432 pin configuration 7432 signetics 74LS 7432 TTL 7432 OR propagation delay 74LS32 specification and configuration logic symbol 74LS32 pin configuration and logic symbol 74LS32 pin configuration of 7432 Text: ï»¿Signetics I 7432, LS32, S32 Gates Logic Products Quad Two-Input OR Gate Product Specification , than or equal to the table entries. VM- 1.3V for 74LS ; VM - 1.5V lor all other TTL families Input , . INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74 74S 74LS A, B Inputs 1ul 1Sul 1LSul Y , Respective Manufacturer Signetics Logic Products Product Specification Gates 7432, LS32, S32 ABSOLUTE , 0.5 0.5 V Iql = 4mA ( 74LS ) 0.25 0.4 V Input clamp IK voltage Vcc - MIN, I, = I|k -1.5

OCR Scan PDF 74LS32 74S32 N7432N, N74LS32N, N74S32N SO-14 N74LS32D, N74S32D 10Sul 10LSul ttl 7432 7432 ttl 7432 pin configuration 7432 signetics 74LS 7432 TTL 7432 OR propagation delay 74LS32 specification and configuration logic symbol 74LS32 pin configuration and logic symbol 74LS32 pin configuration of 7432

**74ls32 equivalent**

Abstract: IC 74LS32 SPECIFICATIONS 74LS32 fan-out ttl 7432 7432 pin configuration specifications of IC 74ls32 supply voltage Text:

Signetics I 7432, LS32, S32 Gates Quad Two-Input OR Gate Product Specification Logic , Manual. INPUT AND OUTPUT LOADING AND FAN-OUT TABLE PINS DESCRIPTION 74 74S 74LS A, B , A In., and a 74LS unit load (LSul) is 20/iA Ijh and -0.4m A In. LOGIC SYMBOL 5-64 LOGIC SYMBOL (IEEE/IEC) 853-0555 81501 Signetics Logic Products Product Specification Gates 7432 , should be less than or equal to the table entries. December 4, 1985 INPUT PULSE REQUIREMENTS

OCR Scan PDF 74LS32 74S32 N7432N, N74LS32N, N74S32N N74LS32D, N74S32D F07SB0S 74ls32 equivalent IC 74LS32 SPECIFICATIONS 74LS32 fan-out ttl 7432 7432 pin configuration specifications of IC 74ls32 supply voltage

**TTL 7486**

Abstract: 74LS86 pin configuration N74LS86N 7486 signetics 74ls ttl 132 74ls86 74LS 74S86 LS86 N7486N Text: ï»¿Signelics I 748Ã³, LS86, S86 Gates Logic Products Quad Two-Input Exclusive-OR Gate Product , Manufacturer Signetics Logic Products Product Specification Gates 7486, LS86, S86 ABSOLUTE MAXIMUM RATINGS , for 74LS ; Vu - 1.5V for all other 1 input Pulse Definition FAMILY INPUT PULSE REQUIREMENTS , Manufacturer Signetics Logic Products Product Specification Gates 7486, LS86, S86 DC ELECTRICAL , l-lpLH-j V0UT y/vÂ«" WF07570S VM - 1, 3 V for 74LS ; VM - 1,5V for all other TTL families. Waveform 1

OCR Scan PDF 74LS86 74S86 N7486N, N74LS86N, N74S86N N74LS86D, N74S86D 10Sul 10LSul WF07570S TTL 7486 74LS86 pin configuration N74LS86N 7486 signetics 74ls ttl 132 74LS LS86 N7486N

# 74LS11 Triple 3-Input AND Logic Gate, 14-Pin PDIP - 7411 | Ampere Electronics

CD4504BE Voltage Level Shifter

74LS11, 74HC11

SKU: 23547

74LS11 Triple 3-Input AND Logic Gate, 14-Pin PDIP – 7411

- High-Speed CMOS Logic
- Operating Voltage: 2 to 6 V
- Compatibility: Input CMOS, Output CMOS

8,00 EGP

Out of stock

- Description
- Reviews (0)

## Description

**74LS11 Triple 3-Input AND Logic Gate, 14-Pin PDIP – 7411**

Texas Instruments standard Logic Gates from the 74LS Family of Low Power Schottky Logic ICs. The 74LS Family use bipolar junction technology coupled with Schottky diode clamps to achieve operating speeds equal to the original 74TTL family but with much lower power consumption

Specifications

Attribute Value Logic Function AND Mounting Type Through Hole Number of Elements 3 Number of Inputs per Gate 3 Schmitt Trigger Input No Package Type PDIP Pin Count 14 Logic Family LS Maximum Operating Supply Voltage 5.25 V Maximum High Level Output Current -

0.4mA Maximum Propagation Delay Time @ Maximum CL 20 ns @ 5 V Minimum Operating Supply Voltage 4.75 V Maximum Low Level Output Current 8mA Maximum Operating Temperature +70 ?C Propagation Delay Test Condition 15pF Length 19.3mm Height 4.57mm Width 6.35mm Minimum Operating Temperature 0 ?C Dimensions 19.3 x 6.35 x 4.57mm

Package Includes:

- 74LS11 Triple 3-Input AND Logic Gate

## Related products

-
-
-
-

# 74LS10 Triple 3-input NAND Gate - Datasheet Hub

The 74LS series of integrated circuits (ICs) was one of the most popular logic families of transistor-transistor logic (TTL) logic chips. 74LS series is a bipolar, low-power Schottky IC. 74LS10 Triple 3-input NAND Gate contain three independent 3-input NAND gates

## 74LS10 Features

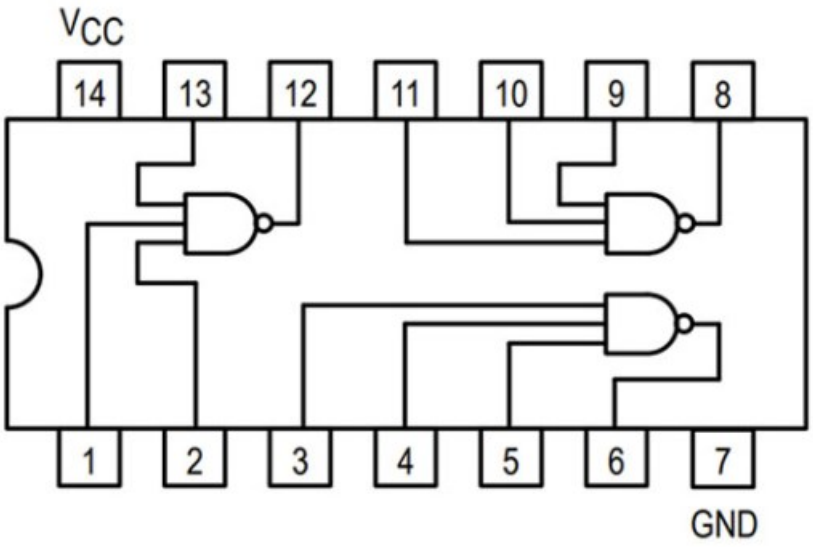
- Three Independent NAND Gates
- Standard Pin Configuration
- Fast Switching Times
- Operating Temperature up to 70°C
- Standard TTL Switching Voltages

## 74LS10 Specifications

Supply Voltage4.75 – 5.25VdcMaximum Clock Frequency40MhzPower Dissipation2mW/gate @100kHzMinimum Output Current8mAPropagation Delay10nSFan Out (TTL Loads)20

## 74LS10 Pinout Diagram

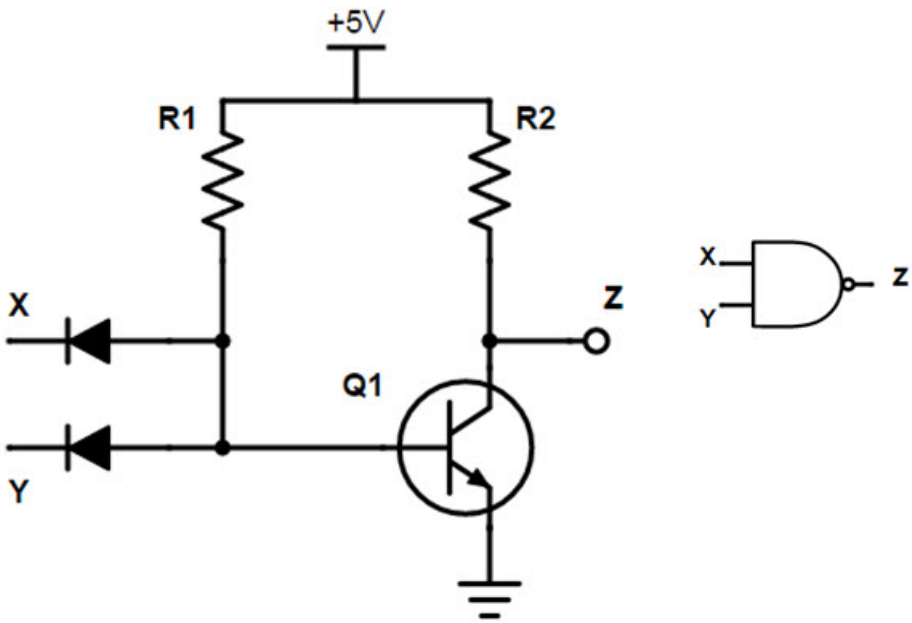
# 74LS10 Pinout




### 74LS10 Pin Description

Pin NoPin NameDescription1A1NAND Gate 1 Input 12B1 NAND Gate 1 Input 23A2 NAND Gate 2 Input 14B2 NAND Gate 2 Input 2 5C2 NAND Gate 2 Input 36D2 NAND Gate 2 Output7GNDGround8D3 NAND Gate 3 Output 9A3 NAND Gate 3 Input 110B3 NAND Gate 3 Input 2 11C3 NAND Gate 3 Input 312D1 NAND Gate 1 Output 13C1 NAND Gate 1 Input 314VCCPositive Supply

## 74LS10 Circuit




### Applications

- Burglar alarm
- Freezer buzzer

**74LS10 Alternative Equivalent**

74LS00, 74LS01, 74LS03

Download 74LS10 Triple 3-input NAND Gate Datasheet from the link given below.

**Related posts:**